## DETAILED ACTION

## EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John P. Wagner on August 29, 2008 (408) 234 3649.

The application has been amended as follows:

IN THE CLAIMS

Claim 1, line 14, replace "wherein said resolving said detected error" by – wherein said resolved said detected error --;

Claim 9, line 16, replace "wherein said resolving said detected error" by – wherein said resolved said detected error --;

Claim 17, line 20, replace "wherein said resolving said detected error" by – wherein said resolved said detected error --;

IN THE SPECIFICATION

Page 21, after page 4, insert – A computer-usable medium having computer-readable program code embodied therein for causing a computer system to perform a method of error protection --;

***Allowable Subject Matter***

2. Claims 1, 3-8, 9, 11-16, 17, 19-24 are allowed.

3. The following is a statement of reasons for the indication of allowable subject matter:

Claims 1, 9, 17 are allowed. Takebe (5257517) discloses when errors frequently take place at a plurality of different locations, issuance of the operation's instruction causes the error display contents to be held (col. 4, lines 55-56); comprising: Realizing data error during communication (col. 5, lines 25-28, when such a data frame signal containing the actuator control data DO as shown in FIG. 5(a) is sent from the main controller 100 to the node 10-1, the data frame signal is sequentially propagated from the node 10-1 via the nodes 10-2, 10-3, 10-4 and to the node 10-5, which results in that the actuator control data DO in the data frame signal are allocated to the corresponding nodes and at the same time the detection data of the sensor group obtained at the respective nodes are taken into the data frame signal); Providing an error indicator at said link when said data error is detected (col. 5, lines 35-45, An error detecting circuit 35 receives the bit Ea in an error signal ERR (refer to FIG. 6) attached to the end of the data frame signal and indicative of the presence or absence of an error and a code CRC in the data frame signal, judges "1" or "0" in the bit Ea to detect the presence or

absence of an error. And the error detecting circuit 35, when the bit Ea is "0", detects the error in the data frame signal through CRC check. When detecting the error in this way, the error detecting circuit 35 inputs a detection signal ED to an error counter 40 and an update enabling signal generating circuit 65. The error counter 40 counts the received detection signal ED and outputs a counted value to the CPU 30); Providing a clear indicator at said link when said data error is resolved (col. 6, lines 15-30, The clear signal generating part 70 generates a clear signal CLR1 to the error counter 40 in accordance with the command received from the CPU 30 and inputs the signal CLR1 to the error counter 40. The clear signal generating part 75 similarly generates a clear signal CLR2 to the error kind register 45 and the error position register 50 in accordance with the command received from the CPU 30 and in puts the signal CLR2 to these registers) (col. 6, lines 40-42, the error kind and position registers 45 and 50 can be updated. More specifically, in this mode, the data of the error kind and position registers 45 and 50 are kept at the previous data until the operator instructs it and when the operator instructs it, the registers are cleared).

Kularatna (6904034) discloses error detection, recovery procedures, notification of unrecoverable errors (col. 4, line 55); comprising: Utilizing a blocking agent at said link to block between said at least two communicating nodes in response to unavailable data transmission (see col. 5, lines 42-45, network service control provides blocking procedure used by NSE to inform a peer NSE when an NS-VC becomes unavailable for data transmission. An unblocking procedure is used to remove the blocking restriction

after the NS-VC become available); utilizing said blocking agent to unblock said blocked communication between said at least two communication nodes.

The prior art however fails to disclose wherein said resolved said detected error comprises generating a clearing bit from each of said communicating nodes, wherein said clearing bits clears a bit in said corresponding position.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571)272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, EDAN ORGAD can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

08/29/08

/Edan Orgad/
Supervisory Patent Examiner, Art Unit 2619